# TS8028N - 100W CW, 500W Peak GaN RF Switch

## 1.0 Features

- Low TX insertion loss: 0.21dB @ 800MHz
- High isolation: 52dB @ 800MHz
- 500W Peak Power Handling
- Versatile 2.6-5.5V power supply
- Operating frequency: 700MHz to 5.0GHz

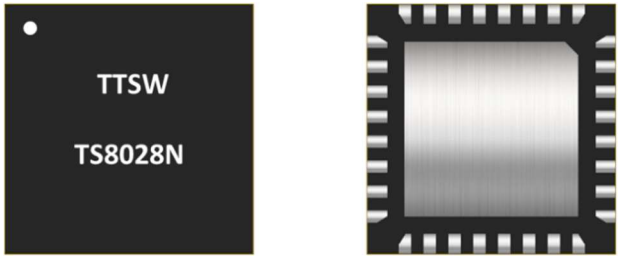



**Figure 1 Device Image**
(32 Pin 5×5×0.85mm QFN Package)

## 2.0 Applications

- Cellular infrastructure
- Small cells
- Macrocells
- ADS-B, IFF Systems

**RoHS/REACH/Halogen Free Compliance**

## 3.0 Description

The TS8028N is an asymmetrical reflective Single Pole Dual Throw (SPDT) switch designed for broadband, high power switching applications. With a simple broadband match, the TS8028N can cover 700MHz to 5.0GHz bandwidth and provide low insertion loss, high isolation and high linearity within a small package size. TS8028N is an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size.

The TS8028N is packaged into a compact Quad Flat No lead (QFN) 5x5mm 32 leads plastic package.

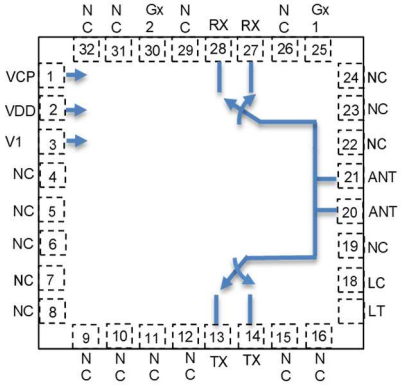



**Figure 2 Function Block Diagram**
(Top View)

## 4.0 Ordering Information

Table 1 Ordering Information

| Base Part Number | Package Type | Form | Qty | Reel Diameter | Reel Width | Orderable Part Number |
|---|---|---|---|---|---|---|
| TS8028N | 32 Pin 5×5×0.85mm QFN | Tape and Reel | 3000 | 13” (330mm) | 18mm | TS8028NMTRPBF |
| Evaluation Board | | | | | | TS8028N-EVB |

## 5.0 Pin Description

Table 2 Pin Definition

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | VCP | Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin. For high duty cycles, higher capacitance is recommended. |
| 2 | VDD | DC power supply |
| 3 | V1 | Switch control input 1 |
| 4,5,6,7,8,9,10,11,16,23,24,31,32 | NC | No internal connection, can be grounded |
| 12,15,19,22,25,30,26,29 | NC | No internal connection. Must be left Open |
| 13,14 | TX | TX Port |
| 17,18 | LT, LC | Tuning Inductor |
| 20,21 | ANT | Antenna Port |
| 27,28 | RX | RX Port |

**Note:** The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias and adequate heat sinking must be used to ensure proper operation and thermal management.

## 6.0 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings** @$T_A$=+25°C Unless Otherwise Specified

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| **Electrical Ratings** | | | |
| Power Supply Voltage | VDD | 2.6 to 5.5 | V |
| Storage Temperature Range | $T_{st}$ | -55 to +125 | °C |
| Operating Temperature Range | $T_{op}$ | -40 to +85 | °C |
| Maximum Junction Temperature | $T_J$ | +140 | °C |
| RF Input Power CW, Tcase=+85°C, 915MHz | TX, ANT | TBD | W |
| RF Input Power Peak, Tcase=+85°C, 915MHz, 1% duty cycle, 1.0msec pulse width | TX, ANT | TBD | W |
| **Thermal Ratings** | | | |
| Thermal Resistance (junction-to-case) – Bottom side | $R_{\theta JC}$ | 3.5 | °C/W |
| Soldering Temperature | $T_{SOLD}$ | 260 | °C |
| **ESD Ratings** | | | |
| Human Body Model (HBM) | Level 1B | 500 to <1000 | V |
| Charged Device Model (CDM) | Level C3 | ≥1000 | V |
| **Moisture Rating** | | | |
| Moisture Sensitivity Level | MSL | 1 | - |

**Attention:**

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 Electrical Specifications

**Table 4 Electrical Specifications** @$T_A$=+25°C Unless Otherwise Specified; VDD=+2.7V; 50Ω Source/Load.

| Parameter | Condition | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Operating frequency | | 700 | | 5000 | MHz |
| Insertion loss, TX | 800MHz | | 0.21 | | dB |
| | 2600MHz (matched) | | 0.37 | | |
| | 3550MHz (matched) | | 0.37 | | |
| | 3950MHz (matched) | | 0.45 | | |
| | 4400MHz (matched) | | 0.46 | | |
| Insertion loss, RX | 800MHz | | 0.37 | | dB |
| | 2600MHz (matched) | | 0.48 | | |
| | 3550MHz (matched) | | 0.51 | | |
| | 3950MHz (matched) | | 0.56 | | |
| | 4400MHz (matched) | | 0.55 | | |
| Isolation ANT-TX | 800MHz | | 21 | | dB |
| | 2600MHz (matched) | | 34 | | |
| | 3550MHz (matched) | | 28 | | |
| | 3950MHz (matched) | | 30 | | |
| | 4400MHz (matched) | | 26 | | |
| Isolation ANT-RX | 800MHz | | 52 | | dB |
| | 2600MHz (matched) | | 38 | | |
| | 3550MHz (matched) | | 34 | | |
| | 3950MHz (matched) | | 33 | | |
| | 4400MHz (matched) | | 33 | | |
| Return Loss RX | 800MHz | | 22 | | dB |
| | 2600MHz (matched) | | 38 | | |
| | 3550MHz (matched) | | 22 | | |
| | 3950MHz (matched) | | 29 | | |
| | 4400MHz (matched) | | 22 | | |
| Return Loss TX | 800MHz | | 20 | | dB |
| | 2600MHz (matched) | | 36 | | |
| | 3550MHz (matched) | | 28 | | |
| | 3950MHz (matched) | | 18 | | |
| | 4400MHz (matched) | | 18 | | |
| P0.1dB CW | 0.1dB compression point, 915MHz | | >100 | | W |
| P0.1dB CW | 0.1dB compression point, 3500MHz | | >100 | | W |
| P Peak | Duty Cycle 16% with 10usec pulse width, 915MHz | | 500 | | W |
| P Peak | Duty Cycle 16% with 10usec pulse width, 3500MHz | | 500 | | W |
| RX P0.1dB CW | 500MHz to 4.0GHz | 39 | 41.5 | | dBm |
| Switching time (RX/TX) | 50% ctrl to 90% of RF value is settled. | | 1.6 / 1.5 | | μs |
| | 50% ctrl to 10% of RF value is settled. | | 1.4 / 1.9 | | μs |
| Rise and Fall time (RX/TX) | 10% to 90% of RF value is settled. | | 0.5 / 0.3 | | μs |
| | 90% to 10% of RF value is settled. | | 1.3 / 0.3 | | μs |

| | | | | | |
|---|---|---|---|---|---|
| Control voltage | Power Supply VDD | 2.6 | 3.3 | 5.5 | V |
| | All control pins high, $V_{ih}$ | 1.0 | 3.3 | 5.25 | V |
| | All control pins low, $V_{il}$ | -0.3 | | 0.5 | V |
| Control current | All control pins low, $I_{il}$ | | 0 | | μA |
| | All control pins high, $I_{ih}$ | | | 7.5 | μA |
| Current consumption, IDD | Active mode (VDD on) | | 160 | 200 | μA |

**Note:**

[1] P0.1dB is a figure of merit.

[2] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

## 8.0 Switch Truth Table

**Table 5 Switch Truth Table**

| V1 | Active RF Path |
|---|---|
| 0 | ANT-RX |
| 1 | ANT-TX |

**Attention:**
[1] VDD should be applied first before V1, otherwise may cause damage to the device.
[2] There is an internal pull-down to ground on V1 control pin, the state at start-up without any control voltage applied will be ANT-RX.

## 9.0 Evaluation Board

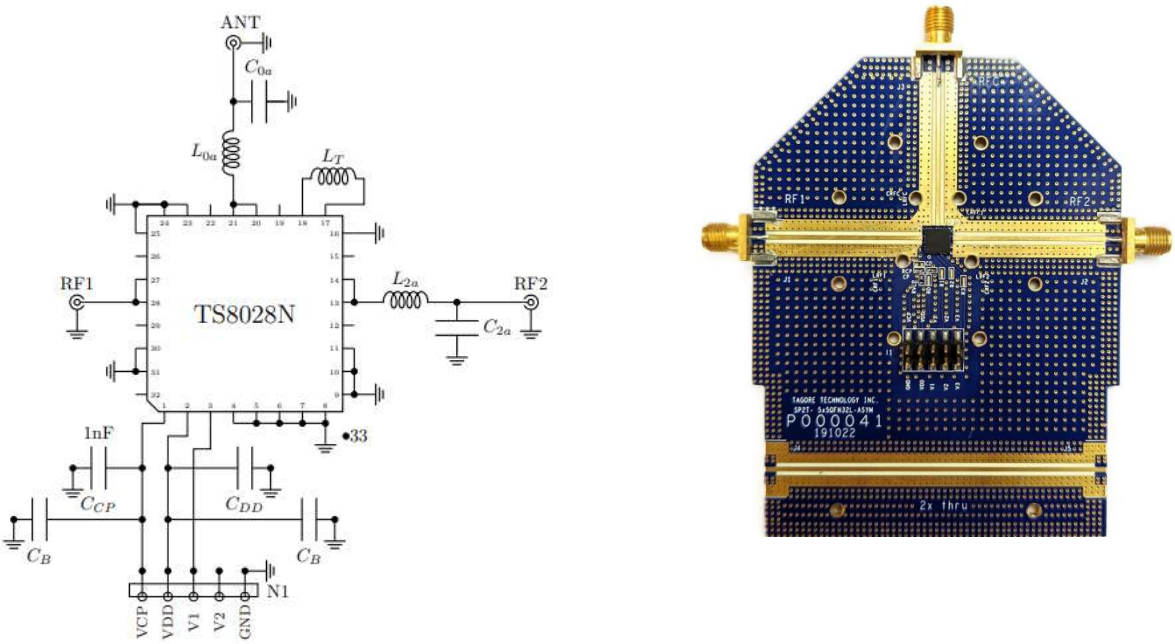



Figure 3 Schematic and evaluation board

**Attention:**
[1] 33 refers to the center pad of the device. Multiple Plugged through hole vias should be added on this Ground Pad and adequate heat sinking should be added.
[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

## 10.1 Typical Characteristics – Unmatched (800 MHz)

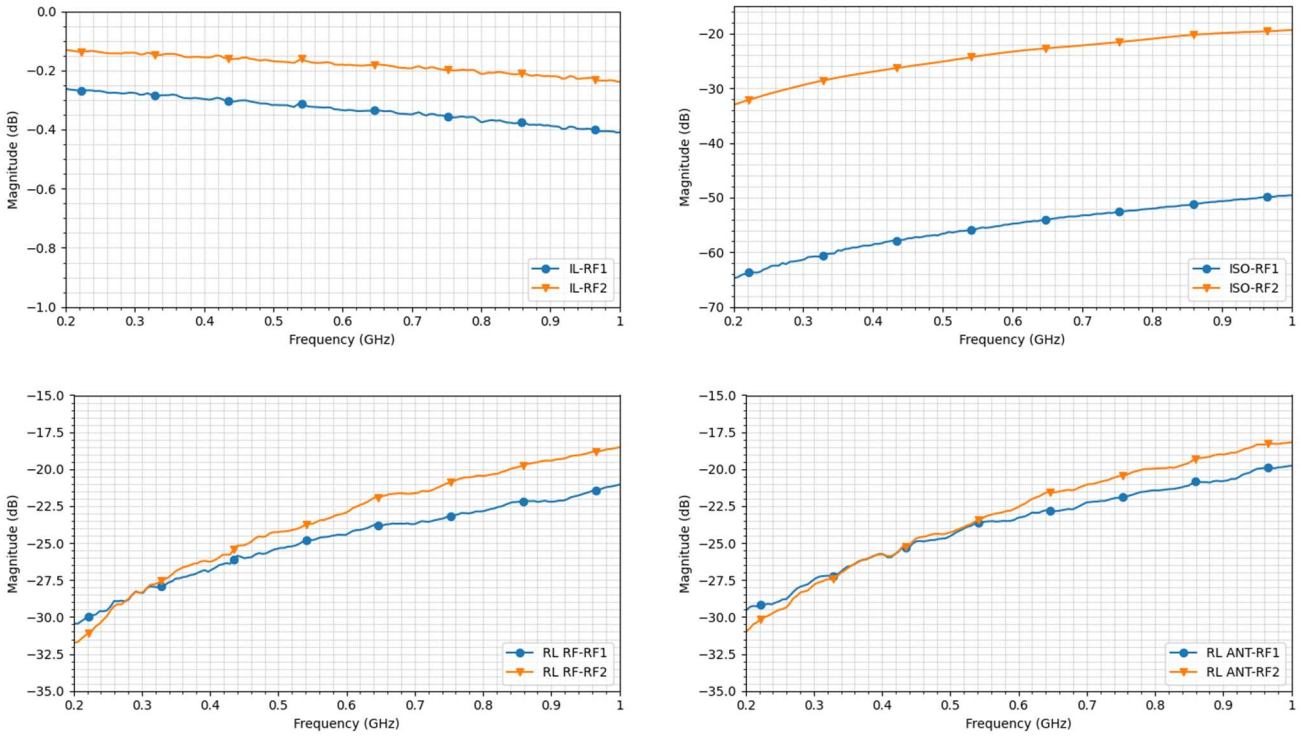



Figure 4.1 Typical characteristics (800 MHz)

## 10.2 Typical Characteristics – Matched (2500 MHz – 2700 MHz)

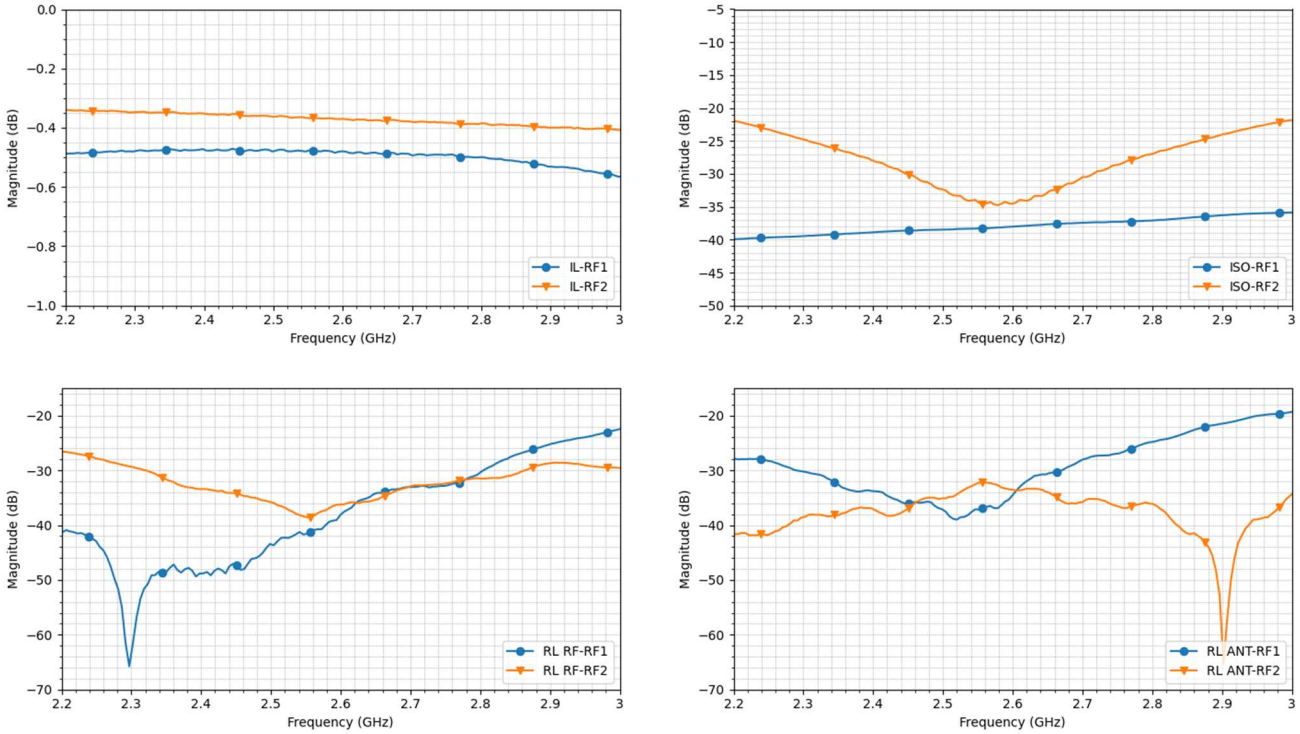



Figure 4.2 Typical characteristics (2500 MHz – 2700 MHz)

## 10.3 Typical Characteristics – Matched (3300 MHz – 3800 MHz)

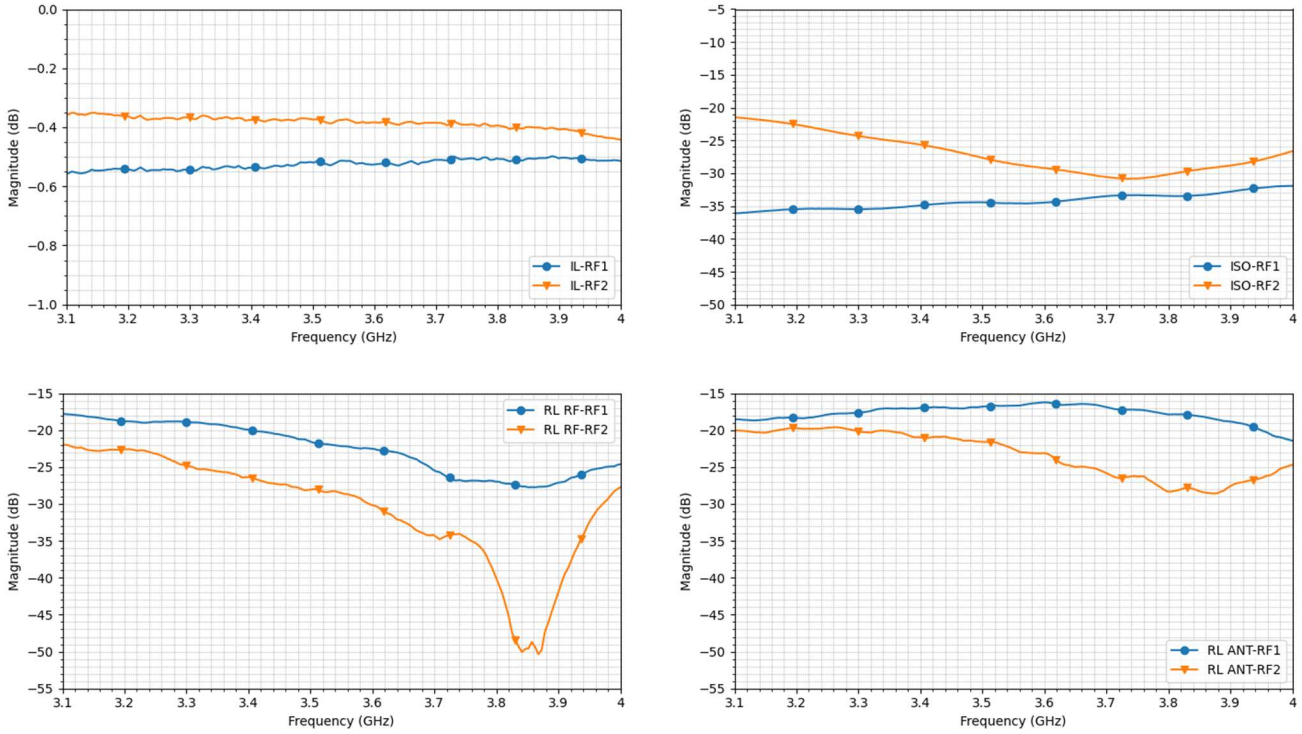



Figure 4.3 Typical characteristics (3300 MHz – 3800 MHz)

## 10.2 Typical Characteristics – Matched (3700 MHz – 4200 MHz)

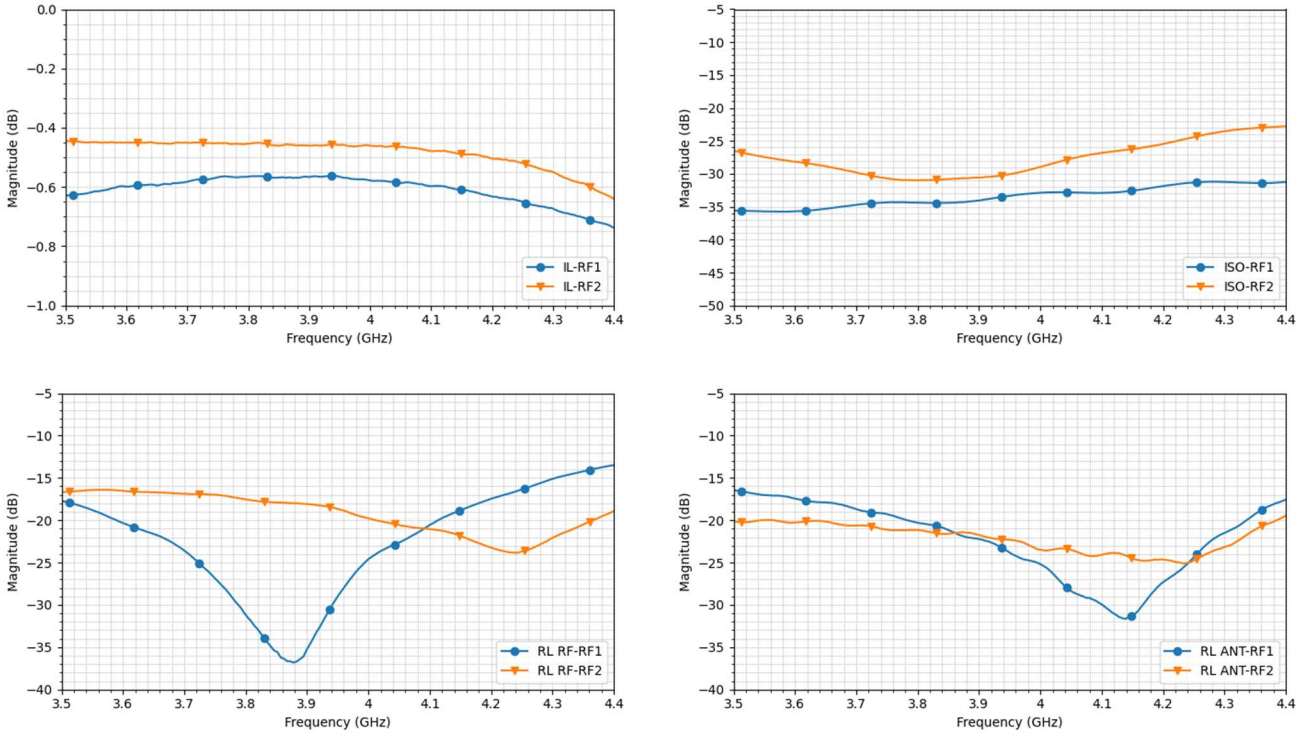



Figure 4.4 Typical characteristics (3700 MHz – 4200 MHz)

## 10.2 Typical Characteristics – Matched (4200 MHz – 4600 MHz)

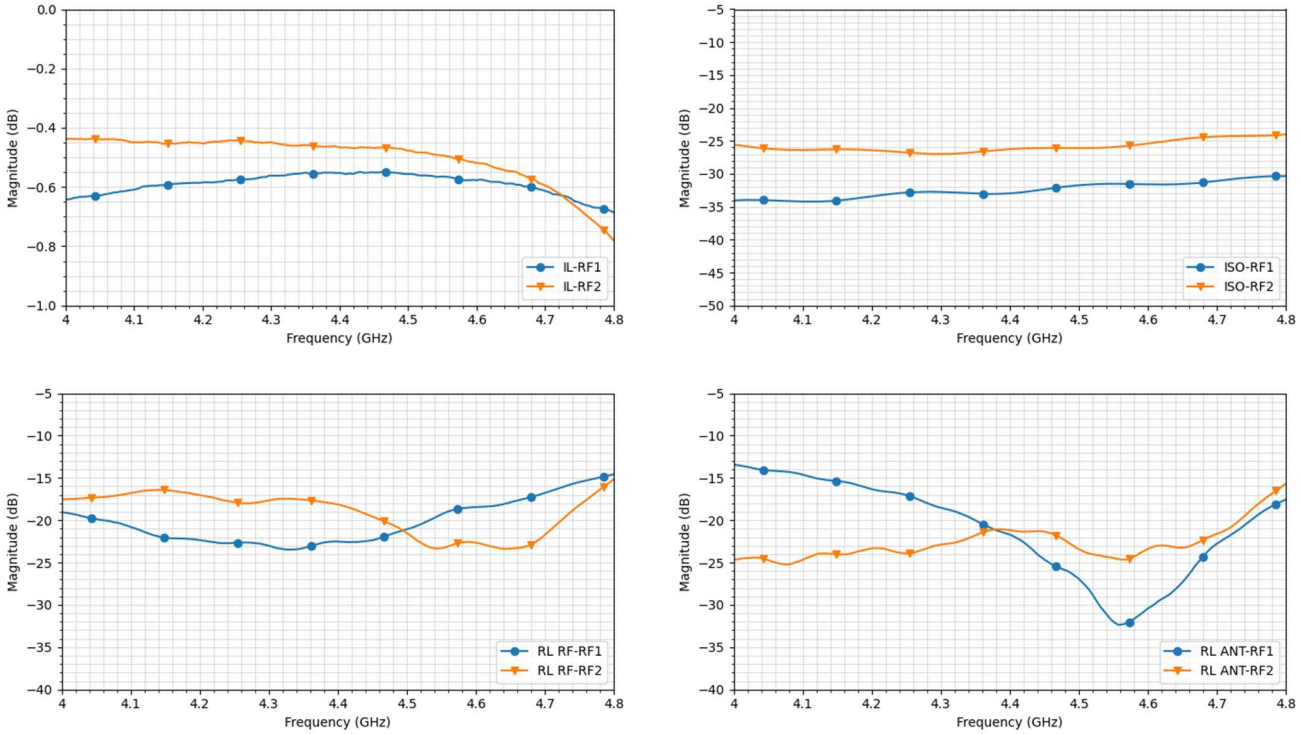



Figure 4.5 Typical characteristics (4200 MHz – 4600 MHz)

## 11.0 Typical Characteristics – Switching Time


Figure 5 Switching Time

## Table 6.1 Bill of Materials – Matching* (800 MHz)

| Component | Part Number | Description | Notes |
|---|---|---|---|
| $C_{CP}$ | GRM155R61E104KA87D | Ceramic capacitor, 0.1 µF, 25 V, ±10%. | |
| $C_{DD}$ | GRM155R71H103KA88 | Ceramic capacitor, 10 nF, 50 V, ±15%. | |
| $L_T$ | | | DNP |
| $L_{0a}$ | | | DNP |
| $C_{0a}$ | | | DNP |
| $L_{2a}$ | | | DNP |
| $C_{2a}$ | | | DNP |

## Table 6.2 Bill of Materials – Matching* (2500 MHz – 2700 MHz)

| Component | Part Number | Description | Notes |
|---|---|---|---|
| $C_{CP}$ | GRM155R61E104KA87D | Ceramic capacitor, 0.1 µF, 25 V, ±10%. | |
| $C_{DD}$ | GRM155R71H103KA88 | Ceramic capacitor, 10 nF, 50 V, ±15%. | |
| $L_T$ | 0402DC-9N0X_R_ | Ceramic core chip inductor, 9.0 nH, ± 5%. | |
| $L_{0a}$ | 0402DC-1N7X_R_ | Ceramic core chip inductor, 1.7 nH, ± 5%. | |
| $C_{0a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF. | |
| $L_{2a}$ | 0402DC-1N7X_R_ | Ceramic core chip inductor, 1.7 nH, ± 5%. | |
| $C_{2a}$ | 0603N0R7BW251 | Ceramic capacitor, 0.7 pF, 250V, ± 0.1pF. | |

## Table 6.3 Bill of Materials – Matching* (3300 MHz – 3800 MHz)

| Component | Part Number | Description | Notes |
|---|---|---|---|
| $C_{CP}$ | GRM155R61E104KA87D | Ceramic capacitor, 0.1 µF, 25 V, ±10%. | |
| $C_{DD}$ | GRM155R71H103KA88 | Ceramic capacitor, 10 nF, 50 V, ±15%. | |
| $L_T$ | 0402DC-4N3X_R_ | Ceramic core chip inductor, 4.3 nH, ± 5%. | |
| $L_{0a}$ | 0402DC-N80X_R_ | Ceramic core chip inductor, 0.8 nH, ± 5%. | |
| $C_{0a}$ | 0603N0R6BW251 | Ceramic capacitor, 0.6 pF, 250V, ± 0.1pF. | |
| $L_{2a}$ | 0402DC-N80X_R_ | Ceramic core chip inductor, 0.8 nH, ± 5%. | |
| $C_{2a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF. | |

## Table 6.4 Bill of Materials – Matching* (3700 MHz – 4200 MHz)

| Component | Part Number | Description | Notes |
|---|---|---|---|
| $C_{CP}$ | GRM155R61E104KA87D | Ceramic capacitor, 0.1 µF, 25 V, ±10%. | |
| $C_{DD}$ | GRM155R71H103KA88 | Ceramic capacitor, 10 nF, 50 V, ±15%. | |
| $L_T$ | 0402DC-3N9X_R_ | Ceramic core chip inductor, 3.9 nH, ± 5%. | |
| $T_{0a}$ ($L_{0a}$) | 4.8 mm | PCB transmission line length. | From the IC-reference plane. |
| $C_{0a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF. | |
| $T_{2a}$ ($L_{2a}$) | 5.5 mm | PCB transmission line length. | From the IC-reference plane. |
| $C_{2a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF. | |

## Table 6.5 Bill of Materials – Matching* (4200 MHz – 4600 MHz)

| Component | Part Number | Description | Notes |
|---|---|---|---|
| $C_{CP}$ | GRM155R61E104KA87D | Ceramic capacitor, 0.1 µF, 25 V, ±10%. | |
| $C_{DD}$ | GRM155R71H103KA88 | Ceramic capacitor, 10 nF, 50 V, ±15%. | |
| $L_T$ | 0402DC-3N2X_R_ | Ceramic core chip inductor, 3.2 nH, ± 5%. | |
| $T_{0a}$ ($L_{0a}$) | 5.4 mm | PCB transmission line length. | From the IC-reference plane. |
| $C_{0a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.4 pF, 250V, ± 0.1pF. | |
| $T_{2a}$ ($L_{2a}$) | 3.5 mm | PCB transmission line length. | From the IC-reference plane. |
| $C_{2a}$ | 0603N0R5BW251 | Ceramic capacitor, 0.5 pF, 250V, ± 0.1pF. | |

* For additional details, please contact the TagoreTech support team.

## 12.0 Device Package Information

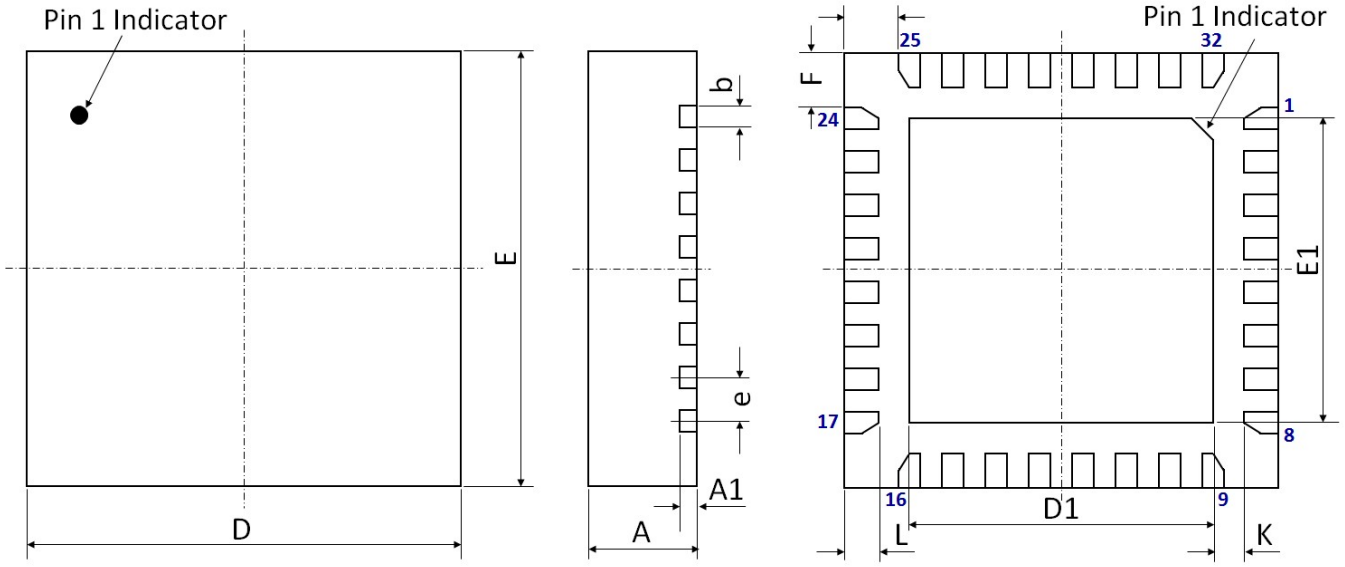



**Figure 28 Device Package Drawing**
(All dimensions are in mm)

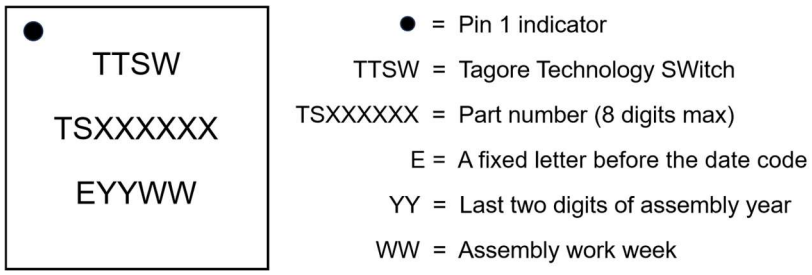
**Table 7 Device Package Dimensions**

| **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) | **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) |
|---|---|---|---|---|---|
| A | 0.85 | ±0.05 | E | 5.00 BSC | ±0.05 |
| A1 | 0.203 | ±0.02 | E1 | 3.20 | ±0.06 |
| b | 0.25 | +0.05/-0.07 | F | 0.625 | ±0.05 |
| D | 5.00 BSC | ±0.05 | G | 0.625 | ±0.05 |
| D1 | 3.20 | ±0.06 | L | 0.40 | ±0.05 |
| e | 0.50 BSC | ±0.05 | K | 0.50 | ±0.05 |

**Note:** Lead finish: Pure Sn without underlayer; Thickness: 7.5μm ~ 20μm (Typical 10μm ~ 12μm)

**Attention:**
Please refer to application notes *TN-001* and *TN-002* at http://www.tagoretech.com for PCB and soldering-related guidelines.

**Top-marking specification:**



## 13.0 PCB Land Design

**Guidelines:**
[1] 4 layer PCB is recommended.
[2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
[3] Thermal vias shall only be placed on the center pad.
[4] The maximum via number for the center pad is 5(X)×5(Y)=25.

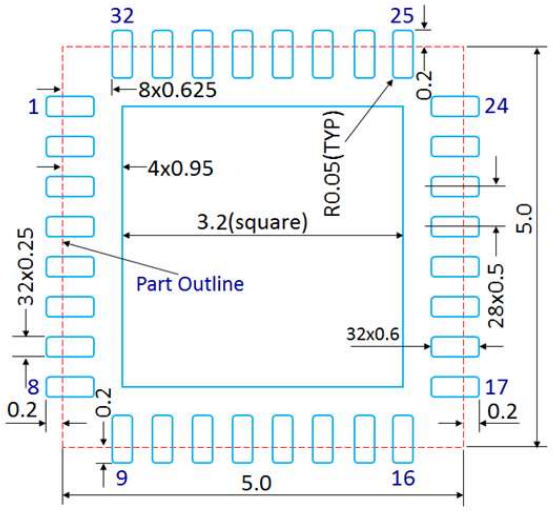
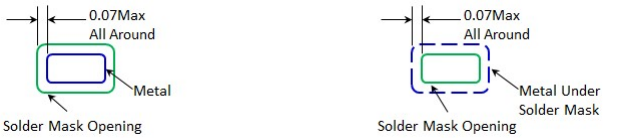



**Figure 29 PCB Land Pattern**
(Dimensions are in mm)




Non-Solder Mask Defined (Preferred)

Solder Mask Defined

**Figure 30 Solder Mask Pattern**
(Dimensions are in mm)

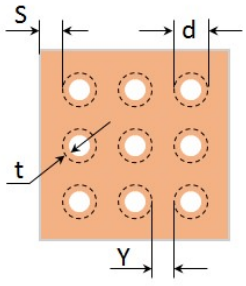



**Figure 31 Thermal Via Pattern**
(Recommended Values: S≥0.15mm; Y≥0.20mm; d=0.2mm; Plating Thickness t=25μm or 50μm)

## 14.0 PCB Stencil Design

**Guidelines:**

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125μm.

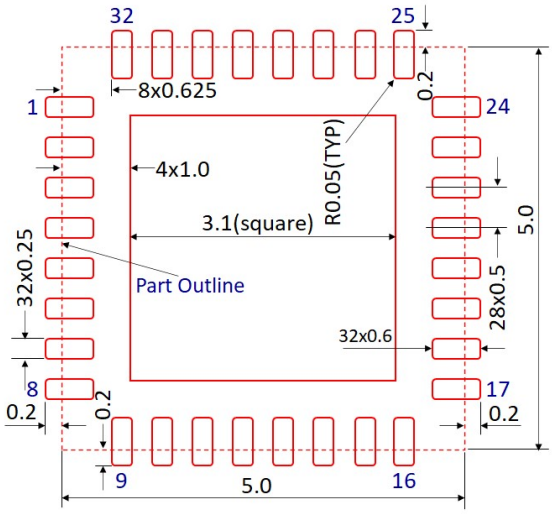



**Figure 32 Stencil Openings**
(Dimensions are in mm)

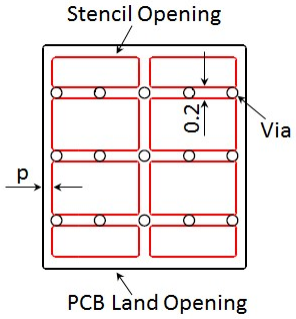



**Figure 33 Stencil Openings Shall not Cover Via Areas If Possible**
(Dimensions are in mm)

## 15.0 Tape and Reel Information

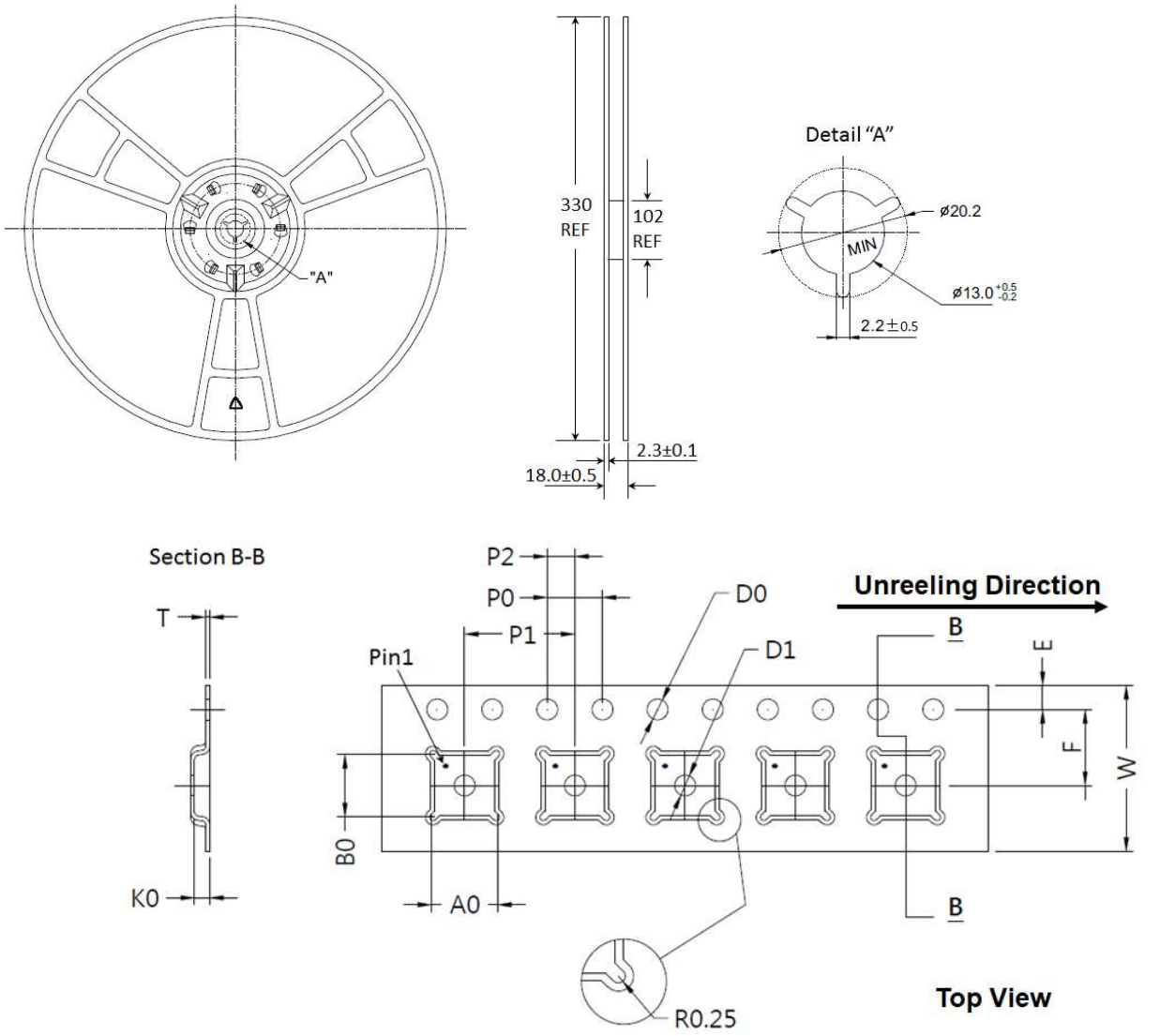



**Figure 34 Tape and Reel Drawing**

**Table 8 Tape and Reel Dimensions**

| **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) | **Dimension** (mm) | **Value** (mm) | **Tolerance** (mm) |
|---|---|---|---|---|---|
| A0 | 5.35 | ±0.10 | K0 | 1.10 | ±0.10 |
| B0 | 5.35 | ±0.10 | P0 | 4.00 | ±0.10 |
| D0 | 1.50 | +0.10/-0.00 | P1 | 8.00 | ±0.10 |
| D1 | 1.50 | +0.10/-0.00 | P2 | 2.00 | ±0.05 |
| E | 1.75 | ±0.10 | T | 0.30 | ±0.05 |
| F | 5.50 | ±0.05 | W | 12.00 | ±0.30 |

**Edition Revision 2.0 - 2024-08-28**

**Published by**
TagoreTech Inc.
601 Campus Drive, Suite C1
Arlington Heights, IL 60004, USA



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